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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,523	06/29/2001	Steven K. Hsu	884.453US1	8095

21186 7590 06/06/2005

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,523	HSU ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims are rejected under 35 U.S.C. 102(e) as being anticipated by Pantelakis et al (6,275,070).

Claim 29, Pantelakis shows a voltage-level converter (Fig. 4) comprising:

A static voltage-level converter including at most four transistors (158, 160, 162, 164) and an inverter (150) coupled to no more than two transistors in the static voltage-level converter each of the no more than two transistors directly coupled to a voltage level (VSSI; and

A split-level output circuit (166) coupled to the static voltage-level converter, wherein the static voltage-level converter includes two down-sized transistors (158, 160, col. 6, lines 55-58).

Claim 30, Pantelakis shows the two down-sized transistors are insulated gate field-effect transistors.

Claim 31, Pantelakis shows a voltage-level converter (Fig. 4) comprising:

A static voltage-level converter including at most four transistors (158, 160, 162, 164) and an inverter (150) coupled to no more than two transistors in the static voltage-level converter each of the no more than two transistors directly coupled to a voltage level (VSSI; and

A split-level output circuit (166) coupled to the static voltage-level converter, wherein the static voltage-level converter comprises:

An input node (CLOCK), a first output node (connected between transistor 158 and 162), and a second output node (RSTCI;

A first pair of transistors connected in series, the first pair of transistors including a first transistor (164) and a second transistors (160), the first transistor coupled to the input node; and

A second pair of transistors connected in series, the second pair of transistors including a first transistor (162) and a second transistor (158), the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors and the second transistor of the second pair of transistors being coupled to the first output node, wherein the inverter (150) is coupled to the input node, to the first transistor of the second pair of transistors, and to the second output node (through 178), wherein the second transistor of the first pair of transistors and the second transistor of the second pair of transistors are down-sized (158, 160, col. 6, lines 55-58).

Claim 32, Pantelakis shows all transistors are insulated gate field-effect transistors.

Response to Arguments

2. Applicant's arguments filed 3/31/05 have been fully considered but they are not persuasive. In response to Applicant's argument that the output circuit 166 of Pantelakis is not a "split-level output circuit", applicant misinterprets the principle that claims are interpreted in the light of the specification. Although these elements (PFET and NFET output are connected in specific way) are found as examples or embodiments in the specification, they were not claimed explicitly. Nor were the words that are used in the claims defined in the specification to require these limitations. A reading of the specification provides no evidence to indicate that these limitations must be imported into the claims to give meaning to disputed terms.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

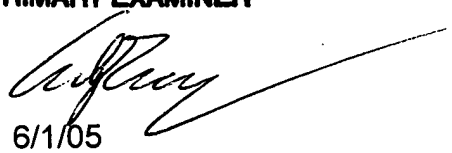
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER



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